Multilevel Inverter-a survey for MV and HV applications

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Abstract— Multilevel inverter (MLI) technology is gaining considerable attention of present research and is a potential rival of conventional Sine wave inverter technology. It however faces limitations of its applications in medium voltage (MV) and High voltage (HV) such as Electrical Power Transmission & Distribution, Medium Voltage (MV) AC motor drives and a few Low Voltage (LV) applications. This is because of large hardware and complex control required for MLI. At low voltage, 2-level PWM Inverters still prevail. Present researches in MLI are towards minimizing hardware and improving upon its performance parameters, and owing to its high Power quality, it could be seen to be replacing 2-level PWM inverters in future. This paper takes thorough review of the Multilevel Inverter topologies, control strategies and its commercial applications as well as recent advancements carried out in this area.

Index Terms— Cascade H-bridge, Inverter, MLI, Modulation, NPC, PWM, switch count, topology, MV Motor drives

1 INTRODUCTION

Many applications such as motor drives, induction heating, High Voltage DC Transmission(HVDC), electricity harnessing from wind, solar PV etc require power electronics conversion stage known as ***Inverter***. A number of topologies have been introduced for inverters. Depending on the output waveform, Inverters are categorized as: square wave Inverter, modified square wave or quasi sine wave Inverter, PWM Inverter and multilevel Inverter. The power quality of first two aforementioned inverters is poor and therefore finds little applications. In sine wave inverter, the power quality is improved by high frequency Pulse-width modulation (PWM) technique. Multilevel Inverter (MLI) technology precludes the necessity of high frequency switching, and forms a staircase AC output by synthesizing input voltages of multiple DC sources, called Levels.

When a large number of DC step levels are synthesized by a proper switching sequence of the inverter solid state switches, the output approaches to sinusoidal with low harmonic content. Hence for High Power- High voltage applications, where the input voltage can be easily divided by means of series connected capacitors, multilevel Inverters are best available alternative. But for medium and low power applications, there is a conflict of opinion. Because of the advantage of compactness (due to few semiconductor switches) and reduced cost, experts of high frequency PWM based Sine wave inverter advocate this technology. On the other hand, low frequency multilevel Inverters experts believe that high efficiency (mainly due to reduced switching power loss), modularity and robustness can be achieved with multilevel Inverter technology only. On one hand, high Voltage inverter applications such as HVDC, FACTS and also MV AC motor drives (from 2.3 to 6.6 kV) have led to the advancement in power semiconductor switches of higher voltage blocking capability which allows the use of conventional PWM Inverter topology in MV motor drives applications to some extent; while on the other hand, new Inverter topology such as MLI was developed to overcome the constraints of voltage and Power ratings of existing power semiconductor switches but at the expense of circuit complexity and higher switch count [1]. In recent years, there have been continuous efforts for minimizing switch count and increasing the efficiency of MLI.

2 THE INVERTER TOPOLOGIES

2.1 The PWM Inverter

It is a 2-level (2L) inverter, which is either voltage sourced (VSI) or current sourced (CSI). In the PWM based VSI, the DC input voltage $V_{dc}$is switched at very fast pace, to the output terminals of the inverter with periodic reversal of polarity. The output voltage thus formed is a chopped square wave of magnitude$\pm V_{dc}$ (Fig.,1b). The AC voltage so produced is different in shape compared to what grid supplies to the consumers i.e., a Sine wave. Hence, the PWM inverter output voltage contains lot of harmonics, which are high frequency ac voltages of low magnitudes. The consequence of these harmonics is increased power loss mainly due to core losses in the electric machines, skin effect in power conductors and result in the

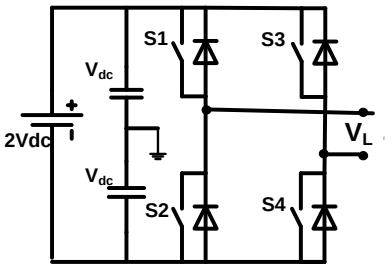

Fig. 1 H-bridge-single phase and its (b)PWM output voltage and (b) load current.

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decreased efficiency.

There are a number of performance parameters for the inverter e.g., total Harmonic distortion (THD), displacement factor (DF), efficiency etc. The fundamental output voltage is the desired sinusoidal output while all high frequency harmonic voltages are unwanted and must be eliminated. THD gives the percent value of combined effective values of all high frequency harmonics to the desired fundamental output. One way to mitigate the harmonics is chopping down the square wave inverter's output at high frequency(up to several KHz), known as Pulse-width modulation (PWM) , that makes the output current nearly sinusoidal for a lagging load, (Fig.1(c)) . The high frequency chopping is only possible if the inverter switches are high speed semiconductor devices e.g., MOSFET, IGBT etc. The H-bridge (single phase full bridge) inverter is a 2-level inverter which requires 4 Power semiconductor switches, while a three phase bridge inverter must have 6 switches. The preferred switching devices for High Power industrial applications are IGBTs, IGCTs and GTOs. However, the maximum blocking voltage capability of the contemporary devices such as IGBT is limited to 6.5kV, 600A and IGCT up to 7.8kV maximum [2] and this also sets the operating voltage limit of conventional 2-level inverters . As the input voltage becomes higher, such as for HVDC and FACTS controllers, the required blocking voltage exceeds the voltage rating of individual switches; and this requires a string of series connected switches in each leg of the inverter. This introduces new problems such as synchronized switching requirement and additional circuits for ensuring voltage and/or current sharing among series connected switches. An alternative solution to this problem is provided by another topology, called Multilevel inverter (MLI)

2.2 The MLI Topology

This has been introduced to overcome limitations of voltage and power rating of semiconductor switching devices. In this topology, a synthesized sinusoidal output voltage as Fig., 2 is produced by connecting various DC source voltages (levels) in additive or subtractive polarity through inverter switches.

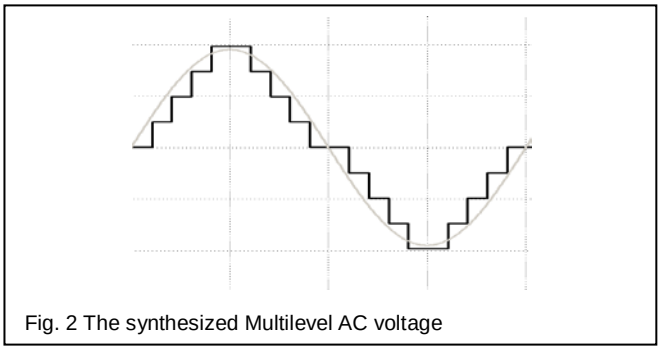

Fig. 2 The synthesized Multilevel AC voltage

Therefore, a number of isolated DC sources or String of charged capacitors, each holding a voltage V_{dc},is required for realizing the desired output. The synthesized staircase AC output voltage so produced has very low distortion which greatly improves the Power quality compared with that obtained by a 2L PWM inverter. Another advantage of MLI is the reduced dv/dt stress, both on inverter switches and load, such as on motor winding insulation. This is due to voltage changes in small steps or levels. This also reduces the Electromagnetic compatibility problems .In addition, the inverter switches can be operated both at the fundamental frequency as well as high switching frequency for PWM. The low frequency switching results in less switching power losses in inverter switches and hence the efficiency is increased. The MLI however, requires large number of switches, which are although of low voltage rating that partially offsets the effect of increased switch count, but each switch requires a separate gate drive circuitry which increases the complexity in circuit and mechanical layout of the inverter.

There are three main topologies so far introduced for MLI: the Diode clamped or Neutral point clamped (NPC), Flying capacitor (FC), and Cascaded H-bridge Multilevel inverter (CMLI). Some others are essentially the combinations of these topologies and termed as hybrid MLI.These are discussed in the next section.

3 REVIEW OF MLI TOPOLOGIES

3.1 NPC or Diode clamped Inverter

The NPC, introduced in 1981 by Nabae et al., is the most popular topology which has been applied to all types of industrial applications up to 6kV [**3**]. The three-level inverter (3L) mainly introduces introduces a 0-volt level to the 2-level inverter output [4]. Later work introduced four and higher-levels inverters for their applications like static VAR compensation, variable speed AC motor drives, and High voltage interconnections [5]. Fig.3**,** shows single phase 3L NPC in which each switch is clamped through diode to the junction of two series connected dc voltage sources (or capacitors) of magnitude V_{dc}. In this way, various voltage levels are tapped to the inverter output terminal through diodes and inverter switches. In general, to form an m-level output, the required number of DC sources (capacitors) is S=m-1 e.g., for a 3-level inverter there are two capacitors required. An m-level three phase Inverter generates

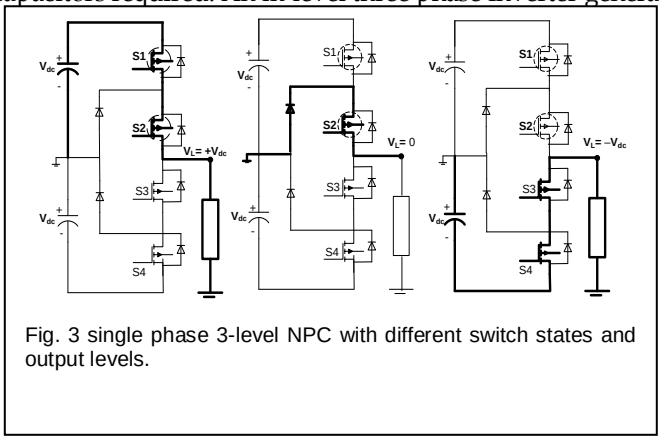

Fig. 3 single phase 3-level NPC with different switch states and output levels.

m-level Phase- neutral voltage and 2m-1 level line- line voltage output. The complete switching states for generating a 3-levels output are shown in Table 1. The topology offers redundancy for 0-volt level as shown in the Table. However, for the selected switch combinations the upper and lower switch pairs such as S1 and S3 , have inverted gate logic. The main advantage of this topology is that the blocking voltage of each switch is restricted by the clamping diode to a level of V_{dc}. However the clamping diodes themselves have unequal block-

TABLE 1
SWITCH STATES FOR 3L NPC, SHOWING REDUNDANCIES FOR 0-VOLTS LEVEL

Inverter output (V_0)	S1	S2	S3	S4
+Vdc	**1**	**1**	**0**	**0**
0	0	1	0	0
0	1	0	1	0
0	**1**	**0**	**0**	**1**
0	0	0	1	0
0	0	0	0	1
-Vdc	**0**	**0**	**1**	**1**
Switch state 1=ON 0=OFF				

ing voltage requirement. This requires either using diodes of different voltage ratings or using string of varying number of symmetric diodes. The converter rating can be increased when more levels are introduced but this also means more inverter switches be employed. Moreover, the number of clamping diodes is related quadratically to m. Hence, for higher levels, the circuit components become too large and layout becomes complex. Table 2 lists the per phase component requirement for NPC Inverter, if diodes and switches are of same voltage rating.

A single switch failure in a string renders the inverter non-operational. Hence for service continuity, a complete redundant inverter is required. Another major drawback of this topology for m>3 , is that the capacitor voltages become unbalanced when the converter phase voltage and line current has in-phase relationship. In this condition, the inner voltage levels of converter output have either current flowing always into or from those particular levels (DC source). This progressively diminishes the respective voltage level. Therefore, an odd level inverter (for instance a 5L converter) operation reduces to a 3L converter and even level inverter converges to a 2L operation. However, for a 90^0 phase relationship between phase voltage and line current, there is no such voltage unbalance problem and this makes the NPC very much suitable for Static Var generation applications. This voltage-unbalance problem can be resolved by using redundant switching states, which are available because of large number of switches present in this topology. For a three phase NPC, there is switch combination more than one that would produce the same output voltage. These redundancies are, however, available for line to line voltage level, but not for Phase voltage [**5**]. For complete voltage balancing another multilevel inverter is required back to back, in which one converter on ac source side, works as rectifier and second, on load side, as Inverter. The DC capacitors corresponding to inner voltage levels of both inverter and rectifier are tied up together. The inner voltage levels capacitors are kept charged from rectifier side as they discharge through inverter and hence the voltage of inner capacitors is balanced [6]. In contrast, the redundant switching states utilization for voltage unbalancing control is only suitable to 3-L NPC. Due to this voltage balancing problem, so far the application of NPC topology has been limited to 3-level inverter for ac motor drives[7],[8],[9] .The 3L NPC also offers the highest converter efficiency and is a preferred choice for many Industrial MV drive systems [10].

An improved version of 3L NPC is active NPC (ANPC), which has been introduced to overcome the unsymmetrical semiconductor-junction temperature distribution [11]. This is caused by the fact that in NPC, the outer switches conduct more than the inner switches and losses are therefore unequal among the switches affecting design of cooling system and puts limits on power rate and switching frequency. In order to give a control over neutral current flow, the clamping diodes are replaced with clamping switches so as to force the neutral current through either upper or lower clamping switch as desired, which would otherwise freewheel via either upper or lower clamping diode based on load voltage polarity preceding to this state, when zero volt level is output by NPC. The NPC has found numerous applications in the market of AC motor drives for conveyers, pumps, fans and mills in oil & gas, metals, Power, mining, hydro, marine, and chemical industry. As this topology can easily employ back to back configuration; it has been applied in the AC drives with regenerative braking, such as regenerative conveyors for the mining industries [12]. It also finds application in interfacing the renewable energy such as wind farms with the grid [13] and also in unified Power flow controller for series and parallel compensation for Transmission Lines [14].

3.2 Flying Capacitor (FC) topology

This topology was introduced by Meynard, & H. Foch [15].It does not require clamping diodes; rather DC side pre-charged capacitors of the inverter are switched in a specific sequence to form the multilevel output voltage. The DC capacitors have stepped structure such that voltage levels held by the outer capacitor leg is greater than the inner capacitors. The step size in the output waveform depends on the voltage level difference between the two adjacent capacitor legs. Fig 4(a) shows the structure of FC MLI for a 4-level Inverter. of switching states which means a particular level can be synthesized by a number of different switch combinations. By virtue of switching redundancies, specific capacitors can be charged/discharged and a control system may utilize this for balancing the voltage levels held by the capacitors [16]. Unlike

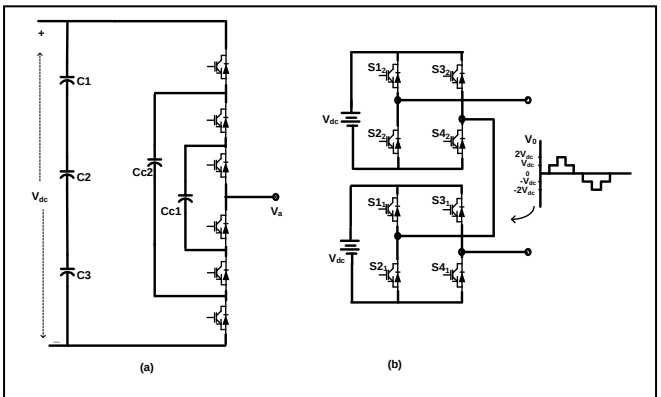

Fig. 4 Single phase 3-level Flying Capacitor (FC) and (b) 5-Level CMLI structure output levels.

NPC, this topology has not found much place in the commercial market because to keep the capacitor voltages balanced, high frequency switching is necessary (≥ 1200 Hz) [17]. Never-

theless, the topology has been successfully implemented in MV drives (4-L FC VSC) as industry standard [7]; it also has made a place in power system such as FACTS and Distributed Generation application [18]

3.3 Cascaded Multilevel Inverter (CMLI)

This is based on chain-link philosophy and is basically composed of series connected H-bridges, each with its own DC source. Hence it is also termed as Cascade H-bridge (CHB) topology. The DC Supply plus H-bridge forms a single cell or link of the so called inverter chain. By virtue of this, the topology is truly modular which facilitates packaging and provides excellent redundancy to the users. Fig.4(b) shows one leg of a three phase 5-level CMLI. Each cell can produce the output voltage- levels of $+V_{dc}, 0$ and $-V_{dc}$ by connecting the input voltage to the load terminals through combination of (diagonally placed) switches such as S1 S4 for $+V_{dc}$; S2 S3 for $-V_{dc}$; and S1 S3 or S2 S4(1 redundant switch state) for 0 volt. The upper and lower switches of each arm have inverted gate Logic to avoid supply short circuit so that $S_1 = \overline{S2}$ and $S_3 = \overline{S4}$.

A Multilevel output can be generated in two ways: either connecting H-bridge cells of equal ratings (symmetrical) or of different ratings (Asymmetric CMLI). For example, by connecting 2 identical Cells in series, there are five output voltage levels: $+V_{dc}, +2V_{dc}, 0, -V_{dc}, -2V_{dc}$. Hence in general, for "N"

TABLE 2
PER PHASE COMPONENTS COUNT FOR VARIOUS MLI TOPOLOGIES

No. of Levels	No. of DC source/Capacitors	No. of Clamping Diodes	No. of balancing Capacitors	No. of active switches with Free-wheeling diodes	Total component count
Neutral Point clamped (NPC)					
m	m-1	(m-1)(m-2)	x	2(m-1)	48
7	6	30	x	12	
Flying Capacitor (FC)					
m	m-1	x	{(m-1)*(m-2)}/2	2(m-1)	33
7	6	x	15	12	
Cascaded H-Bridge(CHB)					
m	½(m-1)	x	x	2(m-1)	15
7	3	x	x	12	
Reduced switch (RSCMLI)					
m	½ (m-1)	x	x	m+2	12
7	3	x	x	9	

x = Not required

number of H-bridge chain-links, output levels in a phase voltage are $2N + 1$ and peak output voltage of NV_{dc} is obtained. For a three phase inverter, line voltage has even higher levels such as $V_{ab} = 9$ levels for the said example and in general $4N + 1$ levels.The numbers of levels in this type of CMLI are linearly related to the number of devices. As each cell provides one redundant switch state, the natural consequence of cascade configuration is to introduce more redundancies with more number of cascaded H-bridge cells for obtaining higher level of output voltage. These redundancies and modularity are the main benefits for fault tolerant operation of this topology [1]. In contrast to NPC and FC topologies, this requires least number of components, as shown in Table 2.

On the other hand, CMLI requires separate DC source for each chain link (H-bridge) and therefore its applications areas are naturally those where multiple DC sources are already available such as traction, Solar PV, and Hybrid renewable sources [19],[20]. For other applications in which multiple DC voltage sources are not available, the DC voltage is formed by a three phase rectifier that is fed by bulky and costly transformer with multiple secondary windings [21]. Due to the requirement of specially designed such large unconventional transformers with multiple phase shifted secondary windings, this topology has been restricted mainly to transformer-less applications such as PV, Battery powered applications. A novel solution has been proposed to overcome this problem in which high frequency transformer with two synchronized converters on input and output side replaces the bulky power transformer [22].

A variation in the topology is the *Asymmetric CMLI* topology that does not require identical cells and more levels can be synthesized from the equal number of circuit components. The maximum resolution or in other words more levels of output voltage is achieved if the DC source voltages of Asymmetric links are related by a ratio of 1:3 [23],[24]. This approach permits lower switching frequency for higher voltage cells and high frequency switching for lower voltage cell [25]. An alternate approach is to think of a CMLI as composed of two inverters: one the main Power conversion unit and the other one as conditioning inverter used as an active filter. The advantage of such configuration is that only one DC supply is required whereas the active filter inverter is supplied by capacitors. In case of fault in the main inverter, the active filter inverter may be used as the main inverter provided that DC source is switched in its circuit. This approach ensures the survivability in Naval ship propulsion loads because they require low power for operation under survival condition [26]

3.4 Hybrid Topologies

These are in essence the combinations of basic topologies. In recent years, several hybrid topologies have been introduced such as transistor clamped converter(TCC), the cascaded NPC , the hybrid NPC-CHB and hybrid FC–CHB topologies. In cascaded NPC, shown in Fig.5, two single phase 3L NPCs form two lags of an H-bridge with input DC capacitors common to both NPCs. In this way 5L output is achieved with only one DC source. The same 5L can also be produced with two series connected conventional H-bridges and require the same number of switches but needs two separate DC sources [27]. A recent extension in another hybrid topology is 5L-ANPC [28]. This combines the 3L-ANPC leg with a 3L-FC power cell that is connected in series with inner ANPC switches. The 3L-FC

cell adds up two more inner levels, making the total levels as equal to 5. Since high levels(>3L) NPC has a potential problem of balancing DC input voltage when active power is taken from it, this hybrid 5L ANPC-FC topology avoids this unbalance as ANPC used here is a 3L inverter. Moreover, this topology also gives the FC a modular design which the basic FC topology lacks[29] The topology has been applied in commercial MV Drives ; see Table 3 . Combining 3L NPC with CHB has evolved yet another hybrid topology[30] in which series connected H-bridge cells (one or two cells) are meant to increase levels but not power as the H-bridges are supplied with floating capacitors and hence no extra active power can be drawn. In essence, CHB act as series connected

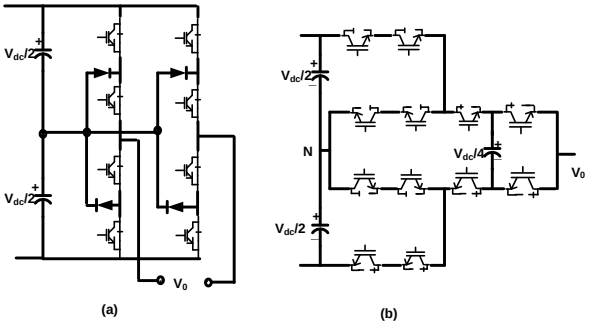

Fig. 5 Hybrid topologies (a) 5LNPC-H-bridge topology (b) 5L ANPC-FC topology

active filters and improve power quality, but introduce additional switch losses and complexity in control circuitry as well. Another important topology, which has been successfully implemented in HVDC is Multilevel Modular converter (MMC). In this topology, single phase, half bridge (2L) cells are series connected in each phase leg. These half bridge cells are split into two equal sections, and therefore, the total cells must be even in number and symmetric positive and negative levels are generated on ac side of the inverter. The main advantage of this topology is its modular structure and the voltage rating can be elevated to Medium to High voltage levels by simply adding more cells in series. One example of such application is 400MW level in which 200 power cell have been used in each phase leg [31].

3.5 New Developments in MLI Topologies

Comparison in Tables 2 reveals that CMLI requires lesser components than the other two topologies and is therefore a preferred topology in most of the cases. However, researchers are still exploring the opportunities for reducing the components count for MLI even further. One such attempt is to use only a single H-bridge (for reversing the polarity) while the DC input voltage is made variable by switching in different combinations of multiple DC voltage sources. In other words, the DC link for this topology is multilevel and main H-bridge is used to invert the polarity of the output voltage. The said topology has been termed as reduced switch cascaded Multilevel Inverter (RSCMLI) [32] Fig.6 shows a 4-level RSCMLI circuit. For conventional CMLI the number of switches N is related to the levels 'm' by N=2(m-1) whereas for RSCMLI topology, the relation N=m+2 holds good and therefore this requires fewer switches, for higher levels m>5, than the conventional topologies.

A recent topology for minimizing the components count of a high quality output uses various number of DC sources arranged with alternately opposite polarity and connected through Power switches to generate various levels [33]. This topology has been termed as MLI based on switched DC sources, which can be applied in applications having multiple DC voltages available, such as, PV modules or multiple renewable sources such as wind plus solar. Compared with the conventional CMLI, the modularity and fault tolerant abilities are little. . However, with respect to components count and losses, this topology is highly competitive to other existing topologies.

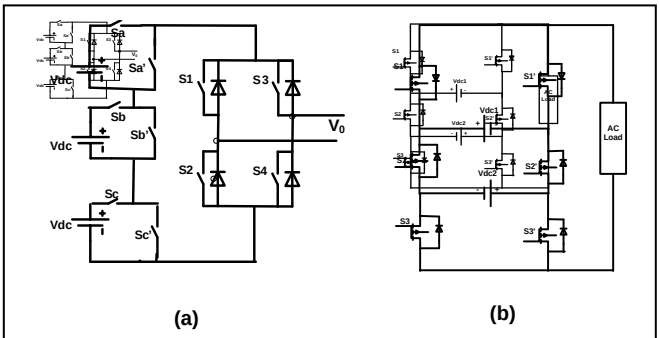

Fig. 6 New topologies (a) Reduced switch CMLI (b) Switched DC source based MLI

4 MODULATION STRATEGIES

The main advantage of MLI topologies is that they can produce a multilevel voltage output by means of fundamental switching frequency. This greatly minimizes switching power loss and results in improved system efficiency. Losses are especially significant for higher power rated switches but less significant for low power switches [34]. Hence to improve the power quality of MLI even further, high frequency PWM strategies have also been applied. The modulation control strategies for MLI are therefore broadly categorized as fundamental switching frequency and high frequency PWM [35]

4.1 Carrier based PWM

This strategy is same as SPWM and requires one reference sinusoidal signal and one carrier per level, except for 0-level. In one approach, these carriers are level shifted, known as level-shifted Multicarrier modulation. For topologies, such as NPC, the high frequency triangular carrier waves are disposed in such a manner that all carriers occupy the adjacent bands to cover full range between maximum levels $+V_{dc}$ and $-V_{dc}$. A single sinusoidal reference signal is then compared with each carrier wave corresponding to a specific level and so determines the switching state of a particular switch corresponding to that level. However, at high modulation index, the DC link utilization is not good [36]. In order to improve this, the sinusoidal reference signal is formed by a third-harmonic injected signal. This does not create any problem as in a three phase inverter, the triplen harmonics or zero sequence components remain absent from the line voltages. This method produces

higher fundamental voltage output without going into over-modulation (ma>1)

Carrier disposition is a well established strategy and can be accomplished for MLI by using three possible methods, as shown in Fig. 7: (i) phase disposition (PD) so that all carriers are in-phase (ii) the carriers below zero axis are 180◦ shifted with respect to those above zero axis, known as Phase opposition disposition (POD), and (iii) alternating the consecutive carriers by 180◦, called Alternate phase opposition-disposition (APOD).In all these strategies, (m-1) carriers are required for m-level Inverter.

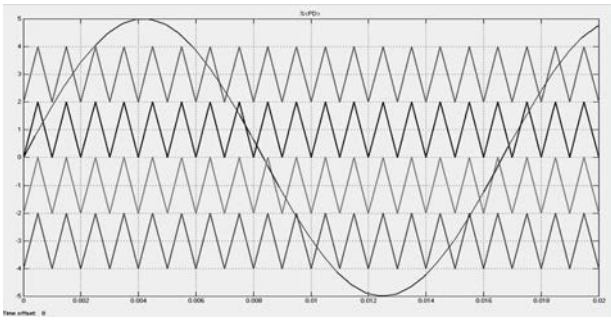

Fig. 7 Level shifted Multicarrier modulation for 5L converter

as each carrier can be easily associated with a particular switch. It is, however, not an attractive technique for CMLI. This is because the uneven power sharing by Cells as a result of less number of switching events in the cells corresponding to intermediate levels results. However, this problem is minimized by modifying the strategy a little; using hybrid switching frequency i.e., carriers with higher frequency for intermediate level cells and low frequency for outer cells [37]. Such an approach would result in evenly power sharing by all cells and prevent unbalance in the separate DC sources of the cascaded cells.

Phase shifted modulation techniques are also successful technique specifically developed for FC and CMLI topologies. Since FC essentially produces a 2 levels output while H-bridge (CMLI) has 3- level output, the modulating strategies using unipolar and bipolar can be applied on CMLI and FC respectively. In both cases, the modulating signal is same for all cascaded H-bridges or FC arms. However, the carrier signal is phase shifted for consecutive cascaded cells by a certain angle. In case of CMLI, it has been demonstrated that a phase shift of 180◦ /N for CMLI and 360◦/N for FC, where N= number of cells. Phase shifted carrier PWM yields the same performance for Cascaded MLI as that produced by APOD for a Diode clamped inverters [38]. By phase shifting the carriers, the harmonics are moved to higher frequency side and this lowers down the requirement of increasing switching frequency (≤ 500Hz) [29]

4.2 Other low frequency modulation techniques

In low frequency modulation techniques, Multilevel selective Harmonic elimination (ML SHE), space vector (SVM) are predominantly employed in various commercial MLIs. Although SPWM technique is classical and easy to implement, but the maximum peak value of the fundamental output voltage is limited to 50% of the input DC link voltage for linear modulation. It is also difficult to extend it to over-modulation range to increase the fundamental output. In contrast, SVM generates more fundamental voltage and less harmonic content. SVM is a pure digital technique in which switch states of the inverter define the space vectors. Each reference voltage vector to be generated is produced by sampling periodically two neighboring space vectors and a null vector. This requires determining the sector (of the so-called space vector hexagon) of that particular reference voltage vector and the duty ratio of sampling the inverter's space vectors. For the case of MLI, this technique involves mapping process between outer and inner sub-hexagonsectors for calculating the switching time duration of various inverter switch vectors. The method becomes quite complex and involve greater computation time in direct proportion to number of levels. A thorough research in this regard introduced new SVM techniques that has successfully reduced this complexity and efforts in computing [39],[40]. These novel techniques, such as 3D SVM, eliminate the requirements of complex calculations of trigonometric functions; look-up Tables or coordinate system transformations. Moreover, these fast computations have same low cost irrespective of the number of levels and hence on line computations can be carried out. Table 3 shows various application areas of commercial MLIs and their features. In most of the applications, Multi Carrier and SVM strategies have been preferred but

TABLE 3
MLI_ APPLICATIONS, TOPOLOGY AND MODULATION TECHNIQUES

Applications	**Power/Topology /Modulation technique**
MV AC Drives	
Siemens Simovert-MV [42]	0.6-7.2 MVA,3.3 kV/3L-NPC,SVM
ABB ACS2000 [44]	280-2200KVA,4kV-6.9kV/5L-ANPC-FC hybrid
TMEIC GE TM drive XL-85	30-120 MVA, 7.2 kV/5L-NPC-HB hybrid
Alstom VDM6000 [43]	0.3-8MVA,4.2kV/4L-FC, PS PWM
General Electric MV-GP-Type H	0.45-7.5 MVA/CHB,PS-PWM
Renewable Energy [29]	
Photovoltaic	NPC/CHB/FC
Wind power	NPC/CHB
Power systems	
FACTS & STATCOM	NPC/ANPC/CHB
HVDC	±800kV,5000MW/MMC
Traction and Automotive	
ABB Wimmis For railway Power 50/16.7 Hz static frequency converter	15-20MW/3L NPC
HE/HEV [29]	CHB/ANPC/FC

some specific applications require other schemes such as Selective Harmonic elimination (SHE)[41]. In this scheme, specific harmonics are eliminated for which computation of switching angles are done off line and stored in look-up Tables. Therefore, this scheme is limited to open loop applications and the converter may not respond to dynamic changes. Moreover, computation of switching angles become complex for more than 5 levels as the number of transcendental equations to solve increase with number of levels.

5 CONCLUSIONS

Multilevel Inverter technology has been elevated from emerging to mature technology. Its benefit to deliver high power quality and sustainability for MV and HV- high power applications gave impetus to exuberant research and development in this area. That is why, MLI is now industry standard for applications such as HVDC, FACTS, Distributed generation and MV AC motor drives. It also has penetrated into LV applications such as EV and HEV taking advantage of availability of multiple DC source in t the form of batteries. Research is still going in the direction of exploring new topologies, optimum utilization of modulation strategies, minimizing the cost and finding avenues for emerging industrial challenges.

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